

**AMENDMENTS TO THE CLAIMS**

Please replace the claims, including all prior versions, with the listing of claims below.

**Listing of Claims:**

1. (Currently amended) A method~~Method~~ for fabricating a semiconductor structure ~~having the steps of, comprising:~~
  - providing a semiconductor substrate ~~(10)~~;
  - providing a plurality of trenches ~~(G11, G12; G21)~~ in the semiconductor substrate ~~(10)~~ using a first hard mask ~~(50)~~, which trenches are arranged offset with respect to one another in rows ~~(r1, r2)~~ and columns ~~(s1, s2, s3)~~;
  - causing the hard mask ~~(50)~~ to recede by a predetermined distance ~~(Δ)~~ with respect to ~~the~~ a trench wall at ~~the~~ a top side ~~(OS)~~ of the semiconductor substrate ~~(10)~~ for ~~the purpose of forming~~ a first hard mask ~~(50')~~ that has been caused to recede;
  - providing an isolation trench structure ~~(ST)~~ in the semiconductor substrate ~~(10)~~ using a second hard mask ~~(HM)~~, the isolation trench structure ~~(ST)~~ subdividing the first hard mask ~~(50')~~ that has been caused to recede along the rows ~~(r1, r2)~~ into strip sections ~~(50<sub>1</sub>', 50<sub>2</sub>', 50<sub>3</sub>')~~ and the strip sections ~~(50<sub>1</sub>', 50<sub>3</sub>')~~ of adjacent rows ~~(r1, r2)~~ being arranged offset with respect to one another;
  - the receding process resulting in a reduction of an overlap region ~~(KB')~~ between two strip sections ~~(50<sub>1</sub>', 50<sub>3</sub>')~~ of adjacent rows ~~(r1, r2)~~ in comparison with an overlap region ~~(KB)~~ which would be present without the receding process;
  - removing the second hard mask ~~(HM)~~; and
  - filling and planarizing the isolation trench structure ~~(ST)~~ with a filling material ~~(FI)~~ using the first hard mask ~~(50')~~ subdivided into the strip sections ~~(50<sub>1</sub>', 50<sub>2</sub>', 50<sub>3</sub>')~~.
  
2. (Currently amended) The method~~Method~~ according to claim 1, ~~characterized in that wherein~~ the trenches ~~(G11, G12; G21)~~ each have a trench capacitor with a corresponding filling ~~(20)~~, which is sunk with respect to the top side ~~(OS)~~ of the semiconductor substrate ~~(10)~~.

3. (Currently amended) ~~The method~~Method according to claim 1 ~~or 2, characterized in that~~wherein the receding process is realized by an isotropic, preferably wet-chemical, etching process, as a result of which ~~the~~a thickness of the first hard mask (~~50~~) that has been caused to recede is reduced in comparison with ~~the~~a thickness of the hard mask (~~50~~).
4. (Currently amended) ~~The method~~Method according to ~~one of the preceding claims, characterized in that~~claim 1, wherein the first hard mask (~~50~~) is composed of silicon nitride.
5. (Currently amended) ~~The method~~Method according to ~~one of the preceding claims, characterized in that~~claim 1, wherein the second hard mask (~~HM~~) is composed of silicon oxide.
6. (Currently amended) ~~The method~~Method according to ~~one of the preceding claims, characterized in that~~claim 1, wherein the filling material (~~FI~~) is composed of silicon oxide.
7. (Currently amended) ~~The method~~Method according to ~~one of the preceding claims, characterized in that~~claim 1, wherein the receding process results in complete elimination of an overlap region (~~KB~~) between two strip sections (~~50<sub>1</sub>'~~, ~~50<sub>3</sub>'~~) of adjacent rows (~~r1~~, ~~r2~~).